REMARKS

In the Official Action mailed **May 8, 2002**, the Examiner reviewed claims 1-10 and 12-19. Claims 1-3, 5-7, 10, and 12 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dea (USPN 5,469,208, hereinafter "Dea") in view of Potu (USPN 5,859,651, hereinafter "Potu"). Claims 4, 9, 13-17, and 19 were rejected under 35 U.S.C. §103(a) as being unpatentable over Dea and Potu and further in view of Abramatic et al. (USPN 4,546,383, hereinafter "Abramatic"). Claim 8 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea and Potu and further in view of Hardiman (USPN 5,926,223, hereinafter "Hardiman"). Claim 18 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea, Potu, and Abramatic, and further in view of Hardiman.

Rejections under 35 U.S.C. §103(a)

Independent claim 1 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea in view of Potu, and independent claim 13 was rejected under 35 U.S.C. §103(a) as being unpatentable over Dea and Potu and further in view of Abramatic.

Applicant respectfully points out that Dea teaches a **compression/decompression accelerator**, which is independent of any additional logic (see Dea FIG. 1, and column 4, lines 37-60). In contrast, the instant application teaches computing the frame difference within a core logic chip, which includes the **north bridge logic and the video logic** (see FIG. 2, index 200 and page 7, line24 to page 8, line 1). Including the video circuitry within the north bridge chip is advantageous because signals between the video logic and the north bridge logic do not have to travel on wires and buses external to the chip. This provides for faster communication than is possible when the video logic is separate from the north bridge chip. There is nothing within Dea or Potu, either

separately or in combination, which would suggest an advantage to including the video circuitry within the north bridge chip.

Accordingly, Applicant has amended independent claims 1 and 13 to clarify that the core logic chip is a north bridge chip that couples the processor to the system bus.

Hence, Applicant respectfully submits that independent claims 1 and 13 as presently amended are in condition for allowance. Applicant also submits that claims 2-10 and 12, which depend upon claim 1, and claims 14-19, which depend upon claim 13 are for the same reasons in condition for allowance and for reasons of the unique combinations recited in such claims. Dependent claims 11 and 20 were previously cancelled.

Version with markings to show changes made

The Claims:

1. (Thrice Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system, wherein the core logic chip is a [semiconductor]north bridge chip that couples the processor to a main memory and a system bus for the computer system; and

storing the difference frame in a memory in the computer system.

13. (Thrice Amended) A method for compressing video data in a computer system, comprising:

receiving a stream of data from a current video frame in the computer system;

computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system, wherein computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame, and wherein computing the difference frame includes computing the difference frame in a core logic chip within the computer system, wherein the core logic chip is a [semiconductor]north bridge chip that couples the processor to a main memory and a system bus for the computer system;

storing the difference frame in a memory in the computer system;

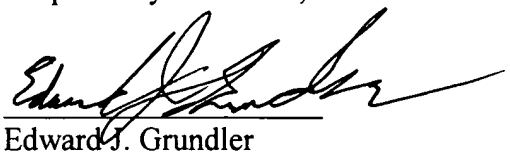
storing the current video frame in the memory in the computer system; and

compressing the video data using the difference frame to produce compressed video data.

CONCLUSION

It is submitted that the present application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

By 

Edward J. Grundler
Registration No. 47,615

Date: July 23, 2002

Edward J. Grundler
PARK, VAUGHAN & FLEMING LLP
508 Second Street, Suite 201
Davis, CA 95616-4692
Tel: (530) 759-1663
FAX: (530) 759-1665